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(54) Low power consumption data transfer bus

Datenübertragung-Bus mit niedrigem Leistungsverbrauch

Bus de transfert de données à consommation d'énergie faible

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Description

[0001] The present invention relates to a circuit arrangement supporting a low power consumption technique and a related method of designing a low power consumption data transfer bus for a circuit arrangement.

[0002] In EP 0 646 873 A2 there is described a microcomputer architecture having three divided internal buses to reduce the load capacity upon the signal transmission path so that signal transmission may be achieved at a high speed.

[0003] Further, in EP 0 600 661 A2 there is described an information processor using an optical storage medium.

[0004] Recently, the introduction of an LSI to a portable device is becoming very popular, and at the same time, there has been a problem of heat generation of an LSI, particularly, of a high performance type. Under these circumstances, there is an increasing demand for the development of an LSI or a VLSI of a low power consumption type.

[0005] An example of effective techniques of achieving a low power consumption is to decrease the power-supply voltage. In general, the power consumption of an LSI or the like is proportional to a square of the power-supply voltage. Therefore, for example, if the power-supply voltage is changed from 5V, which is most widely used at present time, to 3V, which is recently becoming popular, the power consumption decreases to 36% by itself.

[0006] However, if the competition between LSI vendors is taken into consideration, the lowering of the power-supply voltage is only the first step of the low power consumption. In order to meet the demand for the low power consumption, all of the levels of design, from the architecture, functions, circuit technique, to the processing technique, must be satisfied. At each level, effective measurements are, for example, to avoid operating a circuit when it is not necessary (to avoid wasting currents) and to avoid an excessive driving force (proportional to the size of a transistor) for the performance regarding the operation speed.

[0007] Generally, an LSI of a micro-processor, a micro-controller or the like, has a bus capable of transferring data between a plurality of functional blocks. The bus is connected to a number of functional blocks, and in many cases, drawn around in a wide area inside an LSI chip. Thus, the lowering of the power consumption of the bus greatly contributes to the achievement of the low power consumption of the LSI as a whole.

[0008] A conventional example of the low power consumption technique for a bus is a bus dividing method. In this method, one bus is divided into sections by a bus switch circuit, and the bus is operated only when it is needed. As a result, the average load capacitance driven can be decreased, and the power consumption can be lowered.

[0009] However, the mode of the above-described division of the bus is not considered in connection with a specific layout on an LSI chip, and therefore the achievement of the low power consumption is not completely realized. As the worst case, it is necessary to drive all the load on the bus. In this case, the load components situated on another side of the bus switch circuit as viewed from the buffer to drive the load, have to be driven via the bus switch circuit, and therefore the operation speed (data transfer speed) of the bus is decreased as compared to the case where the bus is not divided.

[0010] As described above, according to the conventional data transfer bus, the mode of the division of the bus is not considered in connection with a specific layout on an LSI chip, and therefore the achievement of the low power consumption is not completely realized, and the operation speed (data transfer speed) of the bus is decreased as compared to the case where the bus is not divided.

[0011] The present invention has been proposed as a solution to the above-described problems, and - as defined in claim 1 and 2 - it is achieved by associating the mode of the bus division with a specific layer layout of a circuit arrangement, e.g., an actual LSI chip or an LSI-mounted board layout. The present invention provides a low power consumption data transfer bus, in which the effect of the bus division can be induced to the maximum degree so as to achieve the low power consumption, and the operation speed (data transfer speed) of the bus can be improved as compared to the case where the bus is not divided.

[0012] A low power consumption data transfer bus according to a first aspect of the present invention, includes a bus switch circuit connected so that one data transfer bus provided between a plurality of functional blocks inside an LSI is divided into 3 or more divisional buses. The data transfer bus further comprises a decoder circuit which decodes a control signal which requires two of the three or more divisional buses during an operation, and controls the bus switch circuit so that only the two divisional buses are connected to each other in reply to a decode output.

[0013] A low power consumption data transfer bus according to a second aspect of the invention, includes a bus switch circuit connected so that one data transfer bus provided on a print wiring board on which a plurality of LSIs are mounted, and between the plurality of LSIs is divided into 3 or more divisional buses at one place. The data transfer bus further comprises a decoder circuit which decodes a control signal which requires two of the three or more divisional buses during an operation, and controls the bus switch circuit so that only the two divisional buses are connected to each other in reply to a decode output.

[0014] This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram illustrating a low power consumption data transfer bus according to the first embodiment of the first aspect of the present invention;

FIG. 2A is a circuit diagram illustrating a specific example of a 1-bit section of the bus switch circuit shown in FIG. 1;

FIG. 2B is a circuit diagram which is the same as FIG. 2A when there is no access between the divisional bus 22 and 23.

FIG. 3 is a block diagram illustrating a low power consumption data transfer bus according to the second embodiment of the first aspect of the present invention; and

FIG. 4 is a block diagram illustrating a low power consumption data transfer bus according to the second aspect of the present invention.

[0015] Embodiments of the present invention will now be described in detail with reference to accompanying drawings.

[0016] FIG. 1 is a circuit diagram showing a low power consumption data transfer bus of an LSI according to the first embodiment of the present invention.

[0017] As can be seen in FIG. 1, on an LSI 10 (for example, a micro-controller), a plurality of function blocks 11 to 16 such as a CPU, ROM, RAM and I/O interface, are provided.

[0018] Further, a bus switch circuit 3 is provided, which is connected such that one data transfer bus provided between the plurality of function blocks 11 to 16 within the LSI is divided into 3 or more divisional buses 21 to 23 (in this embodiment, 3).

[0019] Further, a decoder circuit 4 is provided, which serves to a control signal (supplied from the CPU, for example) which requires 2 of the divisional buses 21 to 23 in the operation of the data transfer bus, and control the bus switch circuit such that only the two of the divisional buses are connected to each other at one place on the basis of a decoded output.

[0020] It should be noted that in this embodiment, the number of the bus switch circuit 3 and the decoder circuit 4 is 1, respectively, and the bus switch circuit 3 is located at a predetermined region on the LSI chip 10.

[0021] Loads on the divisional buses 21 to 23 are arranged asymmetrically. Of the plurality of functional blocks 11 to 16, a pair of functional blocks which have the highest average access frequency with respect to the data transfer bus, (for example, CPU and ROM) are connected to one of the divisional buses 21 to 23, which has the smallest load (21 in this embodiment).

[0022] In other words, in FIG. 1, the divisional bus 21, to which a pair of functional blocks which have the highest average access frequency are connected, is constituted so that the load thereon is the smallest under the restriction of the floor layout of the plurality of functional blocks 11 to 16 on the LSI chip 10.

[0023] It should be noted that a load on a divisional bus includes a load component due to wiring, a load component of an output buffer of the functional block for outputting data to the divisional bus, and a load component of an input buffer of the functional block for receiving date from the divisional bus.

[0024] The access frequency to a functional block connected to a divisional bus is defined in the unit of a pair of a functional block for outputting data to the divisional bus and a functional block for receiving data from the divisional bus, and the data of the access frequency can be obtained by operating the LSI in simulation.

[0025] In the structure shown in FIG. 1, the entire power consumption P is proportional to:

$$S = \Sigma F_i \cdot L_i$$

where F_i represents the access frequency of the i-th number of the divisional bus, and L_i represents the load thereon. With this relationship, the minimization of the above $\Sigma F_i \cdot L_i$ will now be considered.

[0026] Supposing that $1 = \Sigma F_i$ and the access frequency of a divisional bus of a smaller number is higher than the access frequency of a divisional bus of a larger number, the following relationship is established:

$$F_i > F_{i+1}$$

[0027] Next, a procedure of carrying out the division of a bus which is close to the optimal for achieving the low power consumption, will now be described.

[0028] First, a pair of functional blocks (the first pair of functional blocks) having the maximum access frequency (the first access frequency) $f_1(=F_1)$ are connected to a first divisional bus 21. Then, in consideration of the layout of the first functional blocks on the LSI chip 10, a layout is made so that the load on the first divisional bus 21 becomes minimum.

[0029] Next, whether a pair of functional blocks (the second pair of functional blocks) having the second maximum access frequency (the second access frequency) f_2 to the maximum access frequency should be connected to the first divisional bus 21, or to a second divisional bus 22, is considered. It should be noted that, if the above two types (the first pair and the second pair) of functional blocks are substantially independent from each other, it is clear by intuitively that the the second pair of functional blocks should be connected to the second divisional bus.

[0030] The case where one of the second pair of functional blocks (for example, CPU) is the same as either one of the first pair of functional blocks, will now be considered. In the relationships provided below, F_1 represents the access frequency to the first divisional bus 21 in the case where the presence of the second pair of functional blocks is not considered (but an area in which it is laid out is maintained), L_1 represents the load ther-

eon, F_2 represents the access frequency to the second divisional bus 22, L_2 represents the load thereon, f represents the access frequency to another block of the second pair of functional blocks, and l_1 and l_2 represents the load appended to the first divisional bus 21 and the second divisional bus, respectively, when the another block is connected to the respective bus.

[0031] The amount which is proportional to the power consumption which increases in the case where the second pair of functional blocks are connected to the first divisional bus 21 is given by:

$$S_1 = (F_1 + f) \cdot (L_1 + l_1) + F_2 \cdot (L_1 + L_2)$$

[0032] In contrast, the amount which is proportional to the power consumption which increases in the case where the second pair of functional blocks are connected to the second divisional bus 22 is given by:

$$S_2 = F_1 \cdot L_1 + (F_2 + f) \cdot (L_1 + L_2 + l_2)$$

[0033] Therefore, the condition for that the power consumption becomes lower if the second pair of functional blocks are connected to the second divisional bus 22, is given by:

$$S_2 - S_1 < 0$$

[0034] That is,

$$(F_2 + f) \cdot l_2 + fL_2 - (F_1 + f) \cdot l_1 < 0$$

$$f \cdot (L_2 + l_2 - l_1) < F_1 \cdot l_1 - F_2 \cdot l_2$$

[0035] It is clear that if the above condition is satisfied, the case where the second pair of functional blocks are connected to the second divisional bus 22 is more effective in terms of the power consumption.

[0036] As the procedure similar to the above is repeated, a bus having a closely minimum power consumption as a whole can be constituted.

[0037] It should be noted that the procedure is one of several methods for constituting a bus having a closely minimum power consumption as a whole.

[0038] Regarding actual micro-computers or the like, in many cases, there is a clear contrast between a functional block pair having a high access frequency and a functional block pair not having such a frequency. Therefore, if the designer of an LSI designs it by trial and error following the above-described procedure, while considering the layout on the LSI chip 10, it is expected that the designer can achieve a closely minimum power consumption without much difficulty.

[0039] However, in the case where there is not a significant difference between functional block pairs in the access frequency, it is expected that the minimum solution for the power consumption cannot be easily found out manually. In order to obtain the minimum solution in a restrict sense, it is necessary to use a mathematical technique for obtaining the minimum solution. In this case, there are an excessive number of parameters to be optimized, and therefore in some cases, the solution becomes a quasi-minimum. In order to avoid this, it is preferable that a method by which a solution close to the minimum can be easily found, such as the simulated annealing method, should be utilized.

[0040] Further, if there is a restriction regarding the operation speed of a bus, such a restriction must also be taken into consideration. However, the bus switch circuit 3 is positioned in one place in order to satisfy the condition by which only the target two types of divisional busses are operated at the same time as described before, and therefore the restriction can be expressed in a simple form. That is, for all of L_i and L_j (i and j are different from each other), the designing should be conducted so that the relationship: $L_i + L_j <$ the upper limit of the load which satisfies the operation speed of the bus, is satisfied.

[0041] Thus, the low power consumption data transfer bus of an LSI, according to the first embodiment, the mode of the bus division is associated with a specific layout on an actual LSI chip 10. With this structure, the effect of the bus division can be obtained to the maximum degree for the achievement of the low power consumption, and the operation speed (data transfer speed) of the bus can be improved to a certain degree as compared to the case where the bus is not divided.

[0042] It is also a possibility that the present invention is used so as to control the power consumption substantially to a possible lower limit, while maintaining the operation speed (data transfer speed) of the bus substantially to a possible upper limit by the divisional bus mode of the present invention. In order to achieve this, pairs of functional blocks which require high bus operating speeds are registered in advance. Then, while executing the above-described flow for achieving the low power consumption, the maximum bus load which satisfy the operation speed is obtained for each of the case where data signal crosses the bus switch circuit, and the case where it does not. Then, each time an appropriate functional block under the condition of the operation speed appears, this functional block should be connected to a predetermined divisional bus with a priority to functional blocks determined in terms of the demand for the achievement of the low power consumption. At any rate, in order to increase the operation speed, it is only natural that a pair of functional blocks which require the most restricted bus operation speed, should be connected to a divisional bus having the smallest load capacity. Note that the above description was made in consideration of that the data transfer which crosses the bus switch circuit generally requires a more time that the

case where the transfer does not cross the circuit. More simply stating, it is possible that if a pair of functional blocks which require a shorter data transfer time, are connected to the same divisional bus, a similar effect can be obtained.

[0043] FIG. 2A shows a specific example of a 1-bit portion of the bus switch circuit 3 shown in FIG. 1. As can be seen in FIG. 2A, a first CMOS switch circuit 31 is connected between a first divisional bus 21 and a second divisional bus 22, a second CMOS switch circuit 32 is connected between the second divisional bus 22 and a third divisional bus 23, and a third CMOS switch circuit 33 is connected between the third divisional bus 23 and the first divisional bus 21.

[0044] In the first CMOS switch circuit 31, a transmission gate made of a first PMOS transistor P1 and a first NMOS transistor N1, is used, in the second CMOS switch circuit 32, a transmission gate made of a second PMOS transistor P2 and a second NMOS transistor N2, is used, and in the third CMOS switch circuit 33, a transmission gate made of a third PMOS transistor P3 and a third NMOS transistor N3, is used.

[0045] A first control signal EN12 used for controlling the connection of the first divisional bus 21 and the second divisional bus 22, is supplied to the gate of the first NMOS transistor N1, and at the same time, after being inverted by a first inverter circuit 34, is supplied to the gate of the first PMOS transistor P1.

[0046] A second control signal EN23 used for controlling the connection of the second divisional bus 22 and the third divisional bus 23, is supplied to the gate of the second NMOS transistor N2, and at the same time, after being inverted by a second inverter circuit 35, is supplied to the gate of the second PMOS transistor P2.

[0047] A third control signal EN31 used for controlling the connection of the third divisional bus 23 and the third divisional bus 21, is supplied to the gate of the third NMOS transistor N3, and at the same time, after being inverted by a third inverter circuit 36, is supplied to the gate of the third PMOS transistor P3.

[0048] Each of the above control signals EN12 to EN31 is set in an active state (level "H" in this embodiment) when corresponding two divisional buses are to be connected, and otherwise set in an inactive state (level "L" in this embodiment).

[0049] It should be noted that each of the CMOS switch circuits 31 to 33 is not limited to a transmission gate as described above, but can be remodeled into some other structure.

[0050] It should be also noted that, as depicted in FIG. 2B, the switch circuit is not necessary between a pair of divisional busses functional blocks connected to one (22) of which have no access between those connected to another (23).

[0051] FIG. 3 shows a low power consumption data transfer bus of an LSI, according to the second embodiment of the first aspect of the present invention.

[0052] The low power consumption data transfer bus shown in FIG. 3 is similar to the data transfer bus shown in FIG. 1 except for the following points. That is, a part of the divisional buses (denoted by reference numeral 23 in this embodiment) is connected so that the part is further divided into three or more divisional buses 232 to 233 by a second bus switch circuit 3a, and functional blocks 17 to 20 are connected to the newly divided buses. Further, a second decoder circuit 4a which corresponds to the second bus switch circuit 3a is provided, and the bus switch circuits 3 and 3a are arranged away from each other on the chip of the LSI. Structural elements shown in FIG. 3, which are similar to those in FIG. 3 are designated by the same reference numerals.

[0053] According to the second embodiment, basically a similar effect to that of the first embodiment can be obtained; however the power consumption increases by the degree corresponding to an increase in the number of elements used. In the case where the pattern area is enlarged if the bus switch circuit is arranged at one place as in the first embodiment, due to the layout on the LSI chip, the increase in the pattern area and the increase in the power consumption trade off with each other. In the case, the second embodiment is recommended to be employed.

[0054] FIG. 4 shows a low power consumption data transfer bus on an LSI-mounted board, according to an embodiment of the second aspect of the present invention.

[0055] The low power consumption data transfer bus shown in FIG. 4 includes a bus switch circuit 43 connected so that one data transfer bus provided between a plurality of LSIs 41 to 46 mounted on a printed wiring board (substrate) 40 is divided into three or more divisional buses. The data transfer bus further includes a decoder circuit 44 for decoding an order signal which requires two of the divisional buses in the operation of the data transfer bus, and for controlling the bus switch circuit so that only the two of the divisional buses are connected to each other in reply to the decode output.

[0056] With the embodiment of the second aspect of the invention, a similar effect to that of the first embodiment of the first aspect of the invention can be obtained by a similar operation.

[0057] As described above, with the low power consumption data transfer bus according to the present invention, the mode of division of a bus is associated with a specific layout on an actual LSI chip or an actual LSI-mounted board, and access frequency between functional blocks connected to the bus and therefore the effect of the bus division can be obtained to the maximum degree for the object of achievement of the low power consumption. Further the operation speed of the bus (that is, data transfer speed) can be improved as compared to the case where the bus is not divided.

Claims

1. Circuit arrangement, comprising:

   a) a plurality of functional blocks (11-16; 41-46);
   b) a data transfer bus provided between said plurality of functional blocks (11-16; 41- 46), said data transfer bus dividing into three or more divisional buses (21, 22, 23; 421, 422, 423);
   c) a bus switch circuit (3; 43) for connecting said plurality of divisional buses to each other; and
   d) a decoder circuit (4; 44) for decoding a control signal which requires two of said plurality of divisional buses during an operation of said data transfer bus, and controlling said bus switch circuit (3; 43) so that only said two divisional buses are connected to each other in reply to a decode output; wherein
   e) the mode of division of the data transfer bus is associated with a specific layout of the functional blocks and with access frequencies between functional blocks connected to the data transfer bus.

2. Circuit arrangement according to Claim 1, **characterized in that** it is a LSI circuit and that said bus switch circuit (3) is positioned in a predetermined section on a chip of said LSI (10) and loads on said divisional buses (21, 22, 23) are asymmetrical.

3. Circuit arrangements according to Claim 1, **characterized by** further comprising:

   a second bus switch circuit (3a) connected so that a part of said divisional buses (21, 22, 23) is further divided into three or more divisional buses (23, 232, 233), wherein said bus switch circuit (3) and said second bus switch circuit (3a) are spaced from each other on the chip of said LSI (10).

4. Circuit arrangement according to Claim 1 or 2, **characterized in that**, of said plurality of functional blocks (11-16), a pair of functional blocks having a highest average access frequency with respect to the data transfer bus are connected to a divisional bus (21) having a lightest load of said plurality of divisional buses (21, 22, 23).

5. Circuit arrangement according to Claim 1, **characterized in that** it is a printed circuit board having a plurality of LSIs (41- 46) mounted therein; and the data transfer bus is provided between said plurality of LSIs.

6. Circuit arrangement according to Claim 1, **characterized in that**, of said plurality of functional blocks (11-16), a pair of functional blocks which require a shortest data transfer time are connected to a divisional bus having a lightest load of said plurality of divisional buses (21, 22, 23).

7. Method of designing a low power consumption data transfer bus for a circuit arrangement comprising a plurality of functional blocks (11-16) being connected by the data transfer bus such that the data transfer bus divides into three or more divisional buses (21, 22, 23) connected by a bus switch circuit (3), wherein:

   a) said plurality of functional blocks (11-16) are registered in order of data transfer time;
   b) a maximum load which satisfies a predetermined data transfer time is obtained both in the case where data crosses the bus switch circuit (3), and the case where data does not cross the bus switch circuit (3);
   c) a pair of functional blocks having the highest average access frequency with respect to the data transfer bus is connected to a divisional bus having the lightest load of said plurality of divisional buses; and
   d) each time a functional block conforming to a condition of said data transfer time appears, said functional block is connected to a predetermined divisional bus prior to a functional block selected according to a power-saving requirement.

Patentansprüche

1. Schaltungsanordnung, die folgendes aufweist:

   a) eine Vielzahl von funktionalen Blöcken (11-16; 41-46);
   b) einen Datenübertragungsbus, der zwischen der Vielzahl von funktionalen Blöcken (11-15; 41- 46) vorgesehen ist, wobei der Datenübertragungsbus in drei oder mehrere Teilbusse (21, 22, 23; 421, 422, 423) aufgeteilt ist;
   c) eine Bus-Umschaltschaltung (3; 43) zum Verbinden der Vielzahl von Teilbussen miteinander; und
   d) eine Decodierschaltung (4; 44) zum Decodieren eines Steuersignals, das zwei der Vielzahl von Teilbussen erfordert, während eines Betriebs des Datenübertragungsbusses, und zum Steuern der Bus-Umschaltschaltung (3; 43), so daß in Antwort auf eine Decodierausgabe nur die zwei Teilbusse miteinander verbunden werden; wobei
   e) die Art einer Teilung des Datenübertragungsbusses mit einem spezifischen Layout der funk-

tionalen Blöcke und mit Zugriffshäufigkeiten zwischen funktionalen Blöcken, die mit dem Datenübertragungsbus verbunden sind, verbunden ist.

2. Schaltungsanordnung nach Anspruch 1, **dadurch gekennzeichnet, daß** sie eine LSI-Schaltung ist und daß die Bus-Umschaltschaltung (3) in einem vorbestimmten Abschnitt auf einem Chip der LSI (10) positioniert ist und Lasten auf den Teilbussen (21, 22, 23) asymmetrisch sind.

3. Schaltungsanordnung nach Anspruch 1, **dadurch gekennzeichnet, daß** sie weiterhin folgendes aufweist:

   eine zweite Bus-Umschaltschaltung (3a), die so angeschlossen ist, daß ein Teil der Teilbusse (21, 22, 23) weiter in drei oder mehrere Teilbusse (23, 232, 233) unterteilt ist, wobei die Bus-Umschaltschaltung (3) und die zweite Bus-Umschaltschaltung (3a) auf dem Chip der LSI (10) voneinander beabstandet sind.

4. Schaltungsanordnung nach Anspruch 1 oder 2, **dadurch gekennzeichnet, daß** von der Vielzahl von funktionalen Blöcken (11-16) ein Paar von funktionalen Blöcken mit einer höchsten durchschnittlichen Zugriffshäufigkeit in bezug auf den Datenübertragungsbus mit einem Teilbus (21) verbunden ist, der von der Vielzahl von Teilbussen (21, 22, 23) eine geringste Last hat.

5. Schaltungsanordnung nach Anspruch 1, **dadurch gekennzeichnet, daß** sie eine gedruckte Schaltungskarte mit einer Vielzahl von LSIs (41- 46) ist, die darin angebracht sind, und der Datenübertragungsbus zwischen der Vielzahl von LSIs vorgesehen ist.

6. Schaltungsanordnung nach Anspruch 1, **dadurch gekennzeichnet, daß** von der Vielzahl von funktionalen Blöcken (11-16) ein Paar von funktionalen Blöcken, die eine kürzeste Datenübertragungszeit erfordern, mit einem Teilbus verbunden ist, der von der Vielzahl von Teilbussen (21, 22, 23) die geringste Last hat.

7. Verfahren zum Entwerfen eines Datenübertragungsbusses mit niedrigem Leistungsverbrauch für eine Schaltungsanordnung, die eine Vielzahl von funktionalen Blöcken (11-16) aufweist, die durch den Datenübertragungsbus so verbunden sind, daß der Datenübertragungsbus sich in drei oder mehrere Teilbusse (21, 22, 23) aufteilt, die durch eine Bus-Umschaltschaltung (3) verbunden sind, wobei:

   a) die Vielzahl von funktionalen Blöcken (11-16) in einer Reihenfolge einer Datenübertragungszeit registriert wird;
   b) eine maximale Last, die eine vorbestimmte Datenübertragungszeit erfüllt, sowohl in dem Fall erhalten wird, in welchem Daten die Bus-Umschaltschaltung (3) kreuzen, als auch dem Fall, in welchem Daten die Bus-Umschaltschaltung (3) nicht kreuzen bzw. überqueren;
   c) ein Paar von funktionalen Blöcken mit der höchsten durchschnittlichen Zugriffshäufigkeit in bezug auf den Datenübertragungsbus mit einem Teilbus verbunden wird, der von der Vielzahl von Teilbussen die geringste Last hat; und
   d) jedesmal dann, wenn ein funktionaler Block, der mit einer Bedingung der Datenübertragungszeit übereinstimmt, erscheint, der funktionale Block mit einem vorbestimmten Teilbus verbunden wird, und zwar vor einem funktionalen Block, der gemäß einem Leistungseinsparerfordernis ausgewählt ist.

Revendications

1. Agencement de circuits comprenant :

   a) une pluralité de blocs fonctionnels (11 à 16 ; 41 à 46) ;
   b) un bus de transfert de données disposé entre lesdits bus de la pluralité de blocs fonctionnels (11 à 16 ; 41 à 46), ledit bus de transfert de données étant divisé en trois bus divisionnaires ou davantage (21, 22, 23 ; 421, 422, 423) ;
   c) un circuit commutateur de bus (3 ; 43) pour connecter ladite pluralité de bus divisionnaires entre eux ; et
   d) un circuit décodeur (4 ; 44) pour décoder un signal de commande nécessitant deux bus de ladite pluralité de bus divisionnaires lors d'une opération dudit bus de transfert de données et commander ledit circuits de commutation de bus (3 ; 43) de façon que seules lesdits deux bus divisionnaires soient connectés l'un à l'autre en réponse à une sortie de décodage ; dans lequel
   e) le mode de division du bus de transfert de données est associé à une implantation spécifique des blocs fonctionnels et à des fréquences d'accès entre les blocs fonctionnels connectés au bus de transfert de données.

2. Agencement de circuits selon la revendication 1, **caractérisé en ce qu'**il est constitué d'un circuit LSI et que ledit circuit commutateur de bus (3) est positionné dans une section prédéterminée sur une puce dudit LSI (10) et les charges sur lesdits bus divisionnaires (21, 22, 23) sont asymétriques.

3. Agencements de circuits selon la revendication 1 ou 2, **caractérisé en ce qu'**il comprend en outre :

un deuxième circuit commutateur de bus (3a) connecté de façon qu'une partie desdits bus divisionnaires (21, 22, 23) soit divisée en outre en trois bus divisionnaires ou davantage (23, 232, 233) dans lequel ledit circuit commutateur de bus (3) et ledit deuxième circuit commutateur de bus (3a) sont espacés l'un de l'autre sur la puce dudit LSI (10).

4. Agencement de circuits selon la revendication 1 ou 2 **caractérisé en ce que**, parmi ladite pluralité de blocs fonctionnels (11 à 16), une paire de blocs fonctionnels ayant une fréquence d'accès moyenne la plus haute par rapport au bus de transfert de données sont connectées à un bus divisionnaire (21) ayant une charge la plus faible de ladite pluralité de bus divisionnaires (21, 22, 23).

5. Agencement de circuits selon la revendication 1, **caractérisé en ce qu'**il s'agit d'une carte de circuit imprimé comportant une pluralité de LSI (41 à 46) montés sur celle-ci ; et le bus de transfert de données est prévu entre les LSI de ladite pluralité de LSI.

6. Agencement de circuits selon la revendication 1, **caractérisé en ce que**, parmi ladite pluralité de blocs fonctionnels (11 à 16), une paire de blocs, fonctionnels nécessitant un temps de transfert de données le plus court sont connectées à un bus divisionnaire ayant une charge la plus faible de ladite pluralité de bus divisionnaires (21, 22, 23).

7. Procédé de conception d'un bus de transfert de données à faible consommation de puissance pour un agencement de circuits comprenant une pluralité de blocs fonctionnels (11 à 16) connectés entre le bus de transfert de Odonnées de façon que le bus de transfert de données soit divisé en trois bus divisionnaires ou davantage (21, 22, 23) connectés par un circuit commutateur de bus (3), dans lequel :

a) ladite pluralité de blocs fonctionnels (11 à 16) sont positionnés dans l'ordre du temps de transfert de données ;
b) une charge maximale satisfaisant à un temps de transfert de données prédéterminé est obtenue à la fois dans le cas où les données passent par le circuit commutateur de bus (3) et dans le cas où les données ne traversent pas le circuit commutateur de bus (3) ;
c) une paire de blocs fonctionnels ayant la fréquence d'accès moyenne la plus élevée par rapport au bus de transfert de donner est connectée à un bus divisionnaire ayant la charge la plus faible de ladite pluralité de bus divisionnaires ; et
d) à chaque fois qu'un bloc fonctionnel se conformant à une condition dudit temps de transfert de données apparaît, ledit bloc fonctionnel est connecté à un bus divisionnaire prédéterminé avant un bloc fonctionnel sélectionné conformément à une exigence d'économie de puissance.

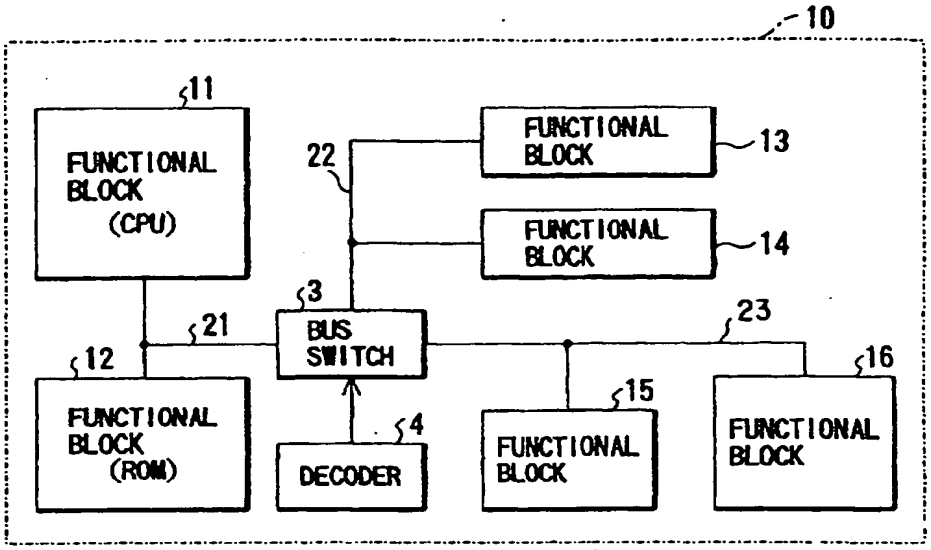
10
11
FUNCTIONAL BLOCK (CPU)
22
FUNCTIONAL BLOCK
13
FUNCTIONAL BLOCK
14
3
BUS SWITCH
21
23
12
16
FUNCTIONAL BLOCK (ROM)
4
DECODER
15
FUNCTIONAL BLOCK
FUNCTIONAL BLOCK

FIG. 1

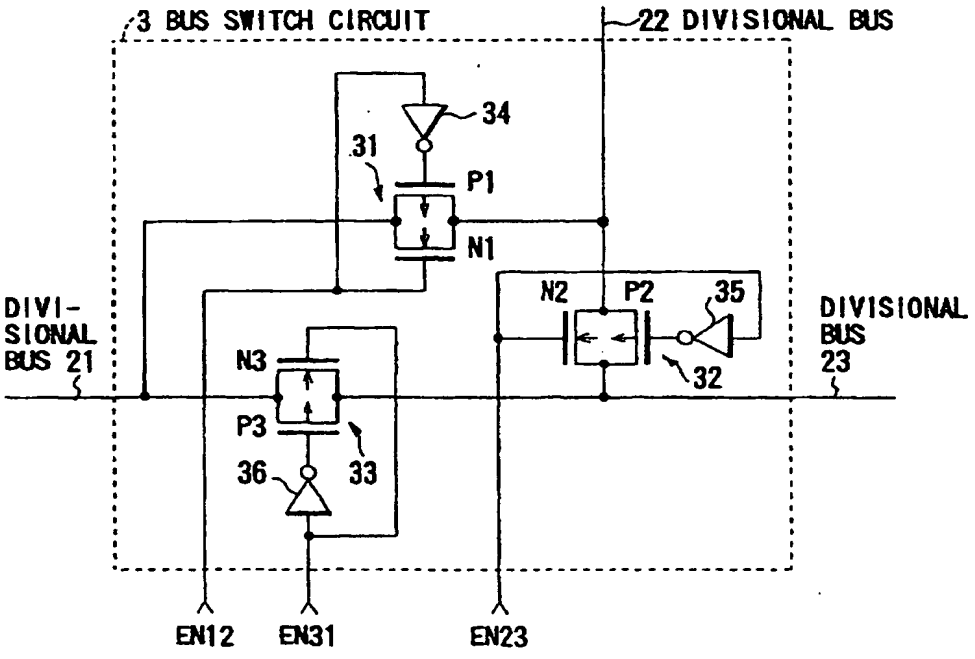
3 BUS SWITCH CIRCUIT
22 DIVISIONAL BUS
34
31
P1
N1
N2
P2
35
DIVI-SIONAL BUS 21
DIVISIONAL BUS 23
N3
32
P3
36
33
EN12
EN31
EN23

FIG. 2A

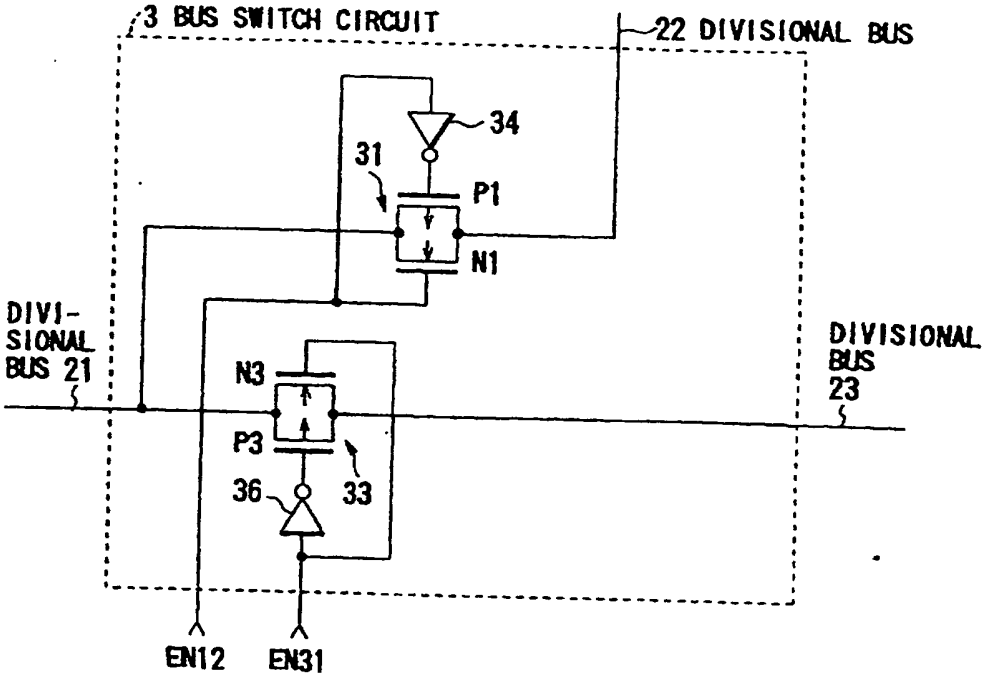
3 BUS SWITCH CIRCUIT
22 DIVISIONAL BUS
34
31
P1
N1
DIVI-
SIONAL
BUS 21
N3
P3
36
33
DIVISIONAL
BUS
23
EN12
EN31

FIG. 2B

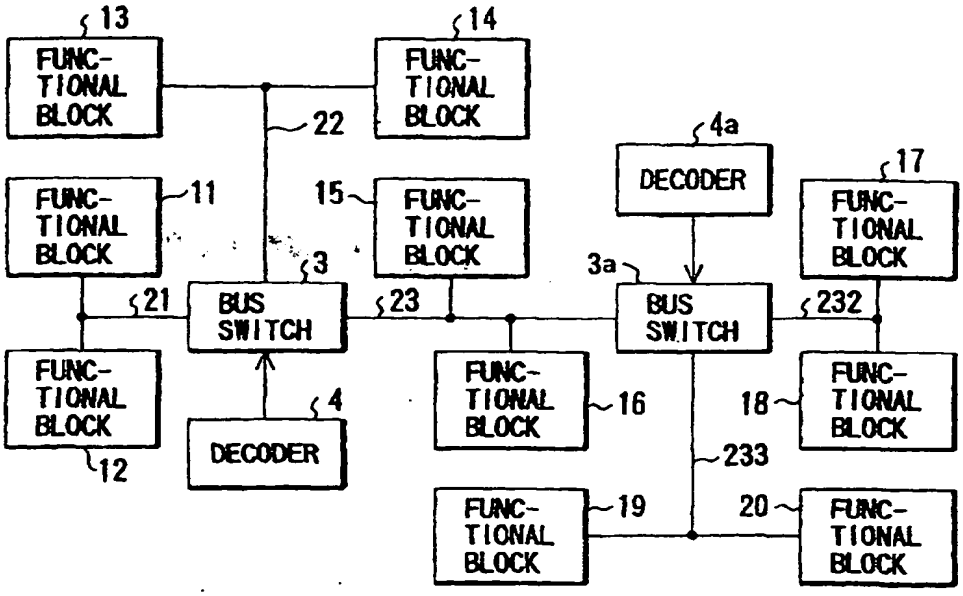
13
FUNC-TIONAL BLOCK
14
FUNC-TIONAL BLOCK
22
4a
DECODER
17
FUNC-TIONAL BLOCK
11
FUNC-TIONAL BLOCK
15
FUNC-TIONAL BLOCK
3
3a
21
BUS SWITCH
23
BUS SWITCH
232
FUNC-TIONAL BLOCK
4
DECODER
FUNC-TIONAL BLOCK
12
FUNC-TIONAL BLOCK
16
18
FUNC-TIONAL BLOCK
233
FUNC-TIONAL BLOCK
19
20
FUNC-TIONAL BLOCK

FIG. 3

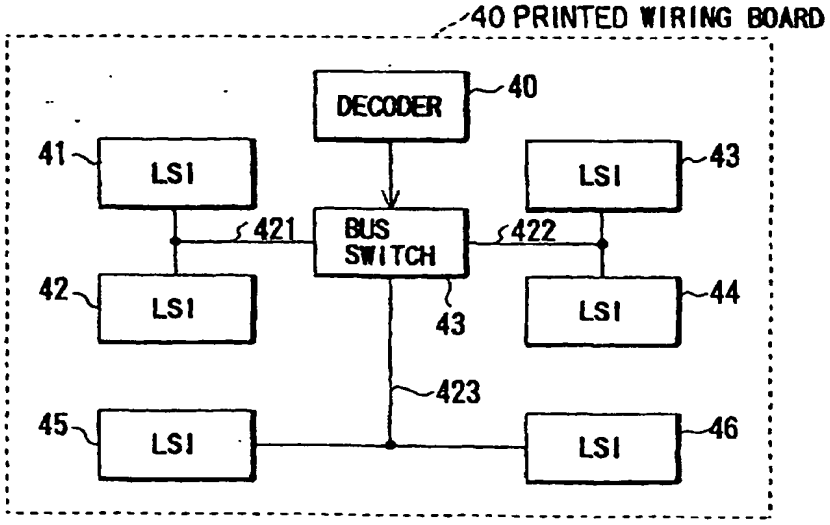
40 PRINTED WIRING BOARD
DECODER
40
41
LSI
LSI
43
421
BUS SWITCH
422
42
LSI
43
LSI
44
423
45
LSI
LSI
46

FIG. 4